IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) A method for fabricating a semiconductor device, the method comprising the steps of:

a) forming a gate insulating film and a gate electrode ~~gateelectrode~~ over a first transistor region defined in a semiconductor substrate;

b) forming, on the semiconductor substrate, a hard mask having an opening for exposing the first transistor region therein, after the step a) has been performed;

c) implanting an impurity into the semiconductor substrate in the manner of large-angle-tilt ion implantation, using the gate electrode and the hard mask as a mask for ion implantation; and

d) removing the hard mask, after the step c) has been performed,

wherein a second transistor region is provided at a side of the first transistor region in part of the semiconductor substrate with an insulating film for transistor isolation interposed therebetween, and

in the step b), the hard mask is formed to cover the second transistor region.

2. (Original) The method of claim 1, wherein in the step b), the thickness of the hard mask and the width of the opening of the hard mask are defined such that the impurity reaches a region under the gate electrode during the large-angle-tilt ion implantation in the step c).

3. (Cancelled)

4. (Original) The method of claim 1, wherein the hard mask is one out of a BPSG film, a PSG film and a silicon nitride film.

5. (Currently amended) ~~The method of claim 1, including the step e) of~~ A method for fabricating a semiconductor device, the method comprising the steps of:

a) forming a gate insulating film and a gate electrode over a first transistor region defined in a semiconductor substrate;

b) forming, on the semiconductor substrate, a hard mask having an opening for exposing the first transistor region therein, after the step a) has been performed;

c) implanting an impurity into the semiconductor substrate in the manner of large-angle-tilt ion implantation, using the gate electrode and the hard mask as a mask for ion implantation;

d) removing the hard mask, after the step c) has been performed; and

e) rounding off an upper edge of the hard mask, thereby making the hard mask to have a tapered edge, between the steps b) and c).

6. (Original) The method of claim 5, wherein in the step e), isotropic etching is performed, thereby making the hard mask to have the tapered edge.

7. (Original) The method of claim 5, wherein in the step e), heat treatment is performed, thereby making the hard mask to have the tapered edge.

8. (Currently amended) A method for fabricating a semiconductor device, the method comprising the steps of:

a) forming a gate insulating film and a gate electrode ~~gateelectrode~~ over a first transistor region defined in a semiconductor substrate;

b) forming a resist layer on the semiconductor ~~thesemiconductor~~ substrate;

c) silylating at least part of the resist layer other than a region of the resist layer located on the first transistor region, thereby forming a silylated region;

d) removing at least part of the region of the resist layer other than the silylated region, thereby forming a silylated resist pattern; and

e) implanting an impurity into the semiconductor ~~thesemiconductor~~ substrate in the manner of large-angle-tilt ion implantation, using the silylated resist pattern as a mask for ion implantation.

9. (Original) The method of claim 8, including the step of oxidizing the silylated region, between the steps d) and e).

10. (New) The method of Claim 5, wherein the hard mask is one of a BPSG film, a PSG film and a silicon nitride film.